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Graphene nanopatterns with crystallographic orientation control for nanoelectronic applications☆☆

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ABSTRACT

The possibility of parallel processing of several features was investigated experimentally for the two methods allowing the crystallographically controlled nanopatterning of graphene: scanning tunneling lithography (STL) and carbothermal etching (CTE). It was found that with multitip systems both methods are suitable for parallel processing. CTE has the advantages that only in the atomic force microscope (AFM) indentation phase is needed the multitip system and it can reveal the location of grain boundaries, so that the nanodevices can be placed in a way that they do not cross grain boundaries. STL is well suited for purposefully producing twisted graphene multilayers with precisely-know misorientations of the individual layers, as also evidenced by Moiré-type patterns observed in the atomic resolution scanning tunneling microscopy (STM) images.

1. Introduction

Graphene, the single atomic layer thick graphite emerged recently, as the very promising, 2D member of the nanocarbons family. Its many exciting properties like the unusual, linear dispersion relation near the Fermi level [1], high thermal conductivity (~5000 $W\,m^{-1}\,K^{-1}$) [2] and large carrier mobility (~200,000 $cm^2\,V^{-1}\,s^{-1}$) [3] brought graphene very quickly to the focus of the attention of many research groups working in the field of nanocarbons. A simple and very ingenious method [4] was proposed by Geim and Novoselov to prepare this material that "should not exist" [1]. A recent review of the field of graphene production enumerates several companies ready to produce tons of graphene [5]. Most of this material is produced by various applications of chemical exfoliation [6], or by using organic solvents to enhance exfoliation [7,8]. Unfortunately even after hydrazine reduction of graphene oxide, some detrimental effects on the electronic properties may persist [9,10]. Thus for nanoelectronic applications the best quality samples are still produced by mechanical exfoliation [4]. Various chemical vapor deposition (CVD) and epitaxial growth processes are also explored to produce high quality graphene. Graphene epitaxy on SiC is a well established method [11,12]; however, here the first graphene layer (also called the zeroth or interfacial layer) interacts strongly with the substrate [13,14]. CVD growth of graphene on Cu [15] is also a promising way of producing large area, high quality sheets. The transfer of the as-grown graphene films to insulating substrates — required for electronic applications — has also been successfully demonstrated [16]. Other metals like Ru [17] and Ni [18] or Ni thin films [19,20] were used as substrates as well. In the CVD material grain boundaries [21] and misoriented layers giving rise to Moiré patterns [22] are expected to play an important role. This aspect has received surprisingly little attention during the increase of interest for graphene until very recently. We showed earlier that point defects, both in carbon nanotubes (CNTs) [23] and in single layers of graphene on SiO_2 [24] produce superstructures in the scanning tunneling microscopy (STM) image, which is a clear indication of the scattering and interference of electronic waves. Therefore a strong effect is expected also in the case of nanodevices crossing grain boundaries in graphene.

Like graphene recently, fullerenes [25] and CNTs [26] generated major turns in research directions all over the world. However, the expectations regarding nanoelectronics have not yet been fulfilled, mainly because of the unsolved problem of placing at acceptable cost levels large numbers of well defined nanoobjects to a specific location with 1 nm, or better, precision. Additional difficulties arise in the case of CNTs due to the still unsolved problem of selecting a specifically requested type of nanotube (either semiconducting or metallic).

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Graphene, due to its sheet-like geometry offers possibilities that fullerenes and CNT are lacking:

- it can cover uniformly large areas with device quality material [12];
- post-deposition electronic structure engineering is possible [27];
- confinement induced gaps that allow room temperature operation can be achieved by scanning tunneling lithography (STL) [28] and tuned by the width of the graphene nanoribbon (GNR); and
- due to its 2D geometry, and the possibility of nanolithography by carbothermal etching (CTE) on SiO_2 [29], it can be integrated with silicon devices, which allows a smooth transition from Si based to C based devices.

Field effect transistors (FETs) outperforming Si devices were already realized from graphene [12], unfortunately these FETs are not suitable for digital applications. Due to the electronic structure of graphene, these transistors do not have an off state. In order to successfully achieve the band gap engineering of graphene, nanometer wide ribbons have to be cut with a very precise crystallographic orientation [28,29].

A crucial issue that may constitute a serious bottleneck, difficult to surpass in the development of graphene based nanoelectronics is the question of parallel lithography. Atomic scale manipulation procedures were already developed in the 1990s, when Eigler and Schweizer realized the IBM logo from Xe atoms on a Ni surface [30], later produced quantum corrals [31], and observed exciting new phenomena, like the quantum mirage [32]. The major difficulty that stopped these types of experiments from turning to technologically relevant applications was that each atom had to be manipulated one by one. This clearly shows that procedures which are able to produce simultaneously multiple features, i.e., parallel processes, are needed.

The present paper compares the two procedures suitable for the production of GNRs with controlled crystallographic orientations of the GNR edges: STL and CTE, under the aspect of parallel processing. The possibility of producing electronically decoupled graphene layers on bulk highly oriented pyrolytic graphite (HOPG) by the rotation of the GNR with respect to the HOPG is investigated. The question of grain boundaries, which will most likely affect any large scale circuit produced from graphene, will be also discussed.

2. Material and methods

For the STL experiments bulk HOPG from commercial suppliers, or few layer graphene (FLG) material produced by mechanical cleavage [4] of HOPG on a gold thin film evaporated on the polished surface of a Si wafer, was used. In order to pattern a single or few layer graphene sheets on the surface of the HOPG, or FLG — used both as material to be patterned and as conductive substrate needed to make the STM operation safe (the deeper layers were acting as a conductive substrate after the topmost layer was cut) — as described in detail earlier [28], we used a commercial Nanoscope III STM operating under ambient conditions. Mechanically prepared Pt–Ir (80:20) tips proved to be the most suitable for both imaging and lithography. First, atomic resolution images were taken on the atomically flat HOPG or graphene sheet. The scan direction was then rotated in order to set the orientation of graphene axes in a convenient direction, and the graphene layer was cut by applying a constant bias potential (significantly higher than the one used for imaging, typically in the range of 2.2–2.6 V) and simultaneously moving the STM tip with constant velocity (1–5 nm/s) in order to etch the desired geometry. Only one single passage of the STM tip over the desired pattern was used. The STM tip was set to ground potential, good results (reproducible cutting, smooth edges) were obtained for positive sample biases. The reaction leading to the patterning of the graphene layer under the STM tip is taking place under conditions far from chemical equilibrium, and is based on the electron beam induced dissociation of the water adsorbed on the HOPG surface, as proposed earlier by McCarley et al. [33]:

$$C + H_2O \Rightarrow CO\uparrow + H_2\uparrow$$

As reported in detail earlier [29] for all our CTE experiments the graphene samples were prepared by micromechanical cleavage [4] from commercial HOPG, and were supported on single crystal silicon wafers having a 90-nm thick SiO_2 top layer. After preparing graphene samples in this way, we exposed them to an oxygen–nitrogen atmosphere at 500 °C. This treatment produces circular etch pits on the graphene surface. This was followed by a subsequent etching step, which consisted of annealing the sample under a continuous flow of Ar gas at 700 °C. After this second treatment step, the circular etch pits produced by oxidation continued to grow in size but were transformed into hexagonal pits with the simultaneous consumption of the substrate SiO_2 according to the reaction:

$$SiO_2 + C = SiO\uparrow + CO\uparrow$$

and importantly no new etch pits were formed. The fact that the etch pits are hexagonal, as opposed to circular, and that they all have the same orientation relative to one another means that the removal of carbon atoms was occurring only at the armchair edges as shown by atomic resolution STM investigations of the sample in the vicinity of the hexagonal holes [29].

3. Results and discussion

3.1. Parallel STL

The experiments for the investigation of the possibilities of parallel STL were carried out on mechanically cleaved FLG samples on Au/SiO_2/Si support. An STM tip with two apexes of equal height was used, which implies that the tunnel current is simultaneously flowing through the two peaks into the sample. These so-called double-tips often form during mechanical tip preparation [34]. In the present experiment the two peaks were situated at a distance of 33.1 nm (as calculated from the distances of the deepest regions of the trenches cut before and after the rotation of the cutting direction) were not isolated from each other.

As shown in Fig. 1c parallel lines separated by 31.25 nm were etched in a reproducible way by the two tips.

However, this distance seems to be too small as in the region between the two tips the surface layer was modified to some extent, as shown in the detailed line cuts in Fig. 1a and b. When the etch direction was rotated by 90° the two tips etched a wider trench, as shown in Fig. 1d and e. One can observe a small but reproducible double well structure of the etched lines, indicating that originally the direction of etching was not rigorously perpendicular to the line joining the two tips.

The results of multiple tip STL show that it is possible to cut nanoscale features in a reproducible way by multiple tips. The width and depth of the etched channels are equally reproducible, the tip positioning system of the STM allows for a very high in plane accuracy even for complex patterns. By carefully planning the switching On/Off of the individual tips, patterns of high complexity can be etched into graphene. It could be convenient to etch the two edges very narrow GNRs with two different tips in subsequent steps. The effective distance between two simultaneously active (etching) tips should be of the order of 50 nm to avoid “cross-talk” in the etching process. Such multitip assemblies could possibly be produced for example from several nanowires [35], or nanorods arranged in parallel and separated by insulating oxide layers. A very promising solution could be the use of anodic Al_2O_3 templates [36]. Of course, a technical solution has to be found for contacting each nanowire individually.

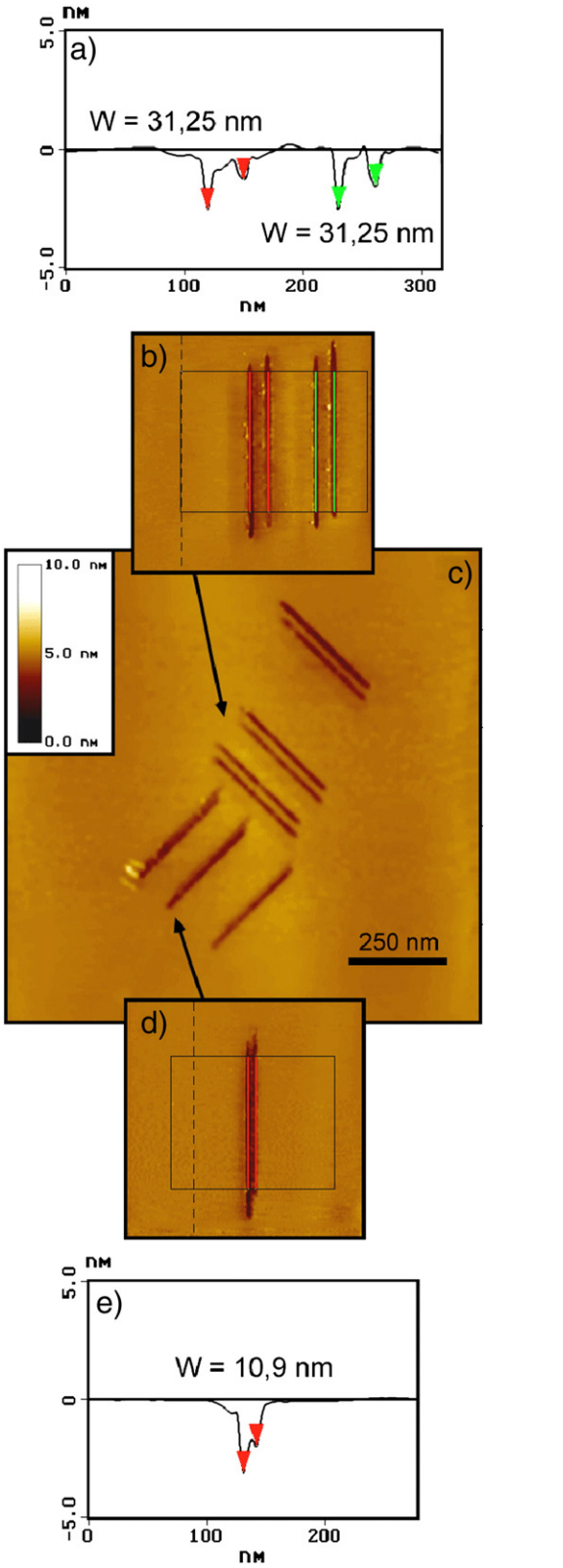

Fig. 1. STM images of GNRs on HOPG etched by a double tip with the two apexes situated about 31 nm apart from each other. By rotating the cutting direction the distance between the cuts made by the two tips can be tuned as apparent from the STM images in subfigures b, c and d for a 90-degree rotation and quantified by the line cuts shown in subfigures a and d.

The STL procedure makes possible the realization of GNRs of widths down to 2.5 nm, like for the GNR shown in Fig. 2. The roughness of the ribbon edges was found to be less than 0.28 nm

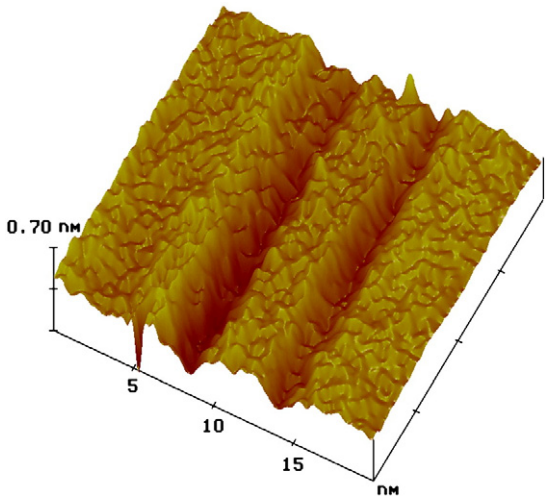

Fig. 2. 3D STM image of a 2.5 nm wide graphene nanoribbon fabricated using the STL method.

(about two carbon atoms). Scanning tunneling spectroscopy (STS) measurements show that armchair GNRs of this width have a band gap of 0.5 eV [28], a value sufficient for the room temperature operation of nanoelectronic devices. With a suitably designed multitip system, patterns of high complexity could be etched within realistic time frames.

3.2. Moiré patterns and layer decoupling

The relative orientation of graphene layers may be important not only under the aspect of grain boundaries, i.e., with respect to neighboring grains, but also with respect to the orientation of the layer(s) below the topmost layer [37]. Recent theoretical calculations show that the interlayer coupling is dependent on the misorientation of the layers [38]. In spite of the weak interaction between graphene layers, many features of this system are determined by interaction conditions between the two layers. It is demonstrated [38] that while the Dirac cones from each layer are always effectively degenerate, the Fermi velocity v_F of the Dirac cones decreases as $\theta \rightarrow 0°$, where θ is the angle of rotation between the layers (Fig. 10 in Ref [38]). For $\theta < 5°$ the Dirac bands become strongly warped as the limit $\theta \rightarrow 0°$ is approached, while at $\theta = 0°$ one has the twofold degeneracy of the *AB* stacked bilayer. As an interesting consequence the bilayer electronic structure will, in general, depend only on the misorientation angle of the layers and not on the details of the real space unit cell. Thus the twisted graphene bilayer encompasses a wide range of electronic behavior, from essentially graphene-like (monolayer) behavior for large angle rotations to quite different behavior in the small angle limit which, nevertheless, shares important features with the large angle case [38]. STL offers a very convenient tool for the detailed investigation of the phenomena arising from twisted multilayers. As we reported earlier, STL is suitable to cut and investigate single layers of graphene [39]. After patterning nanostructures into the top layer of a HOPG crystal by STL, it is also possible to fold-out the fabricated structures, by using the STM tip as a manipulation tool. In order to do so, we have applied severe imaging conditions, characterized by small tip-sample distance, therefore generating strong tip-sample interactions. In Fig. 3, a back-folded single layer graphene flake (see line profile below) is shown. The back-folded flake can be further rotated by using the STM tip as described above. In this way the crystallographic orientation of both layers can be precisely known and even controlled to some extent. In the position shown in Fig. 3b a Moiré pattern with a periodicity of 0.31 nm was observed (average over ten maxima) in

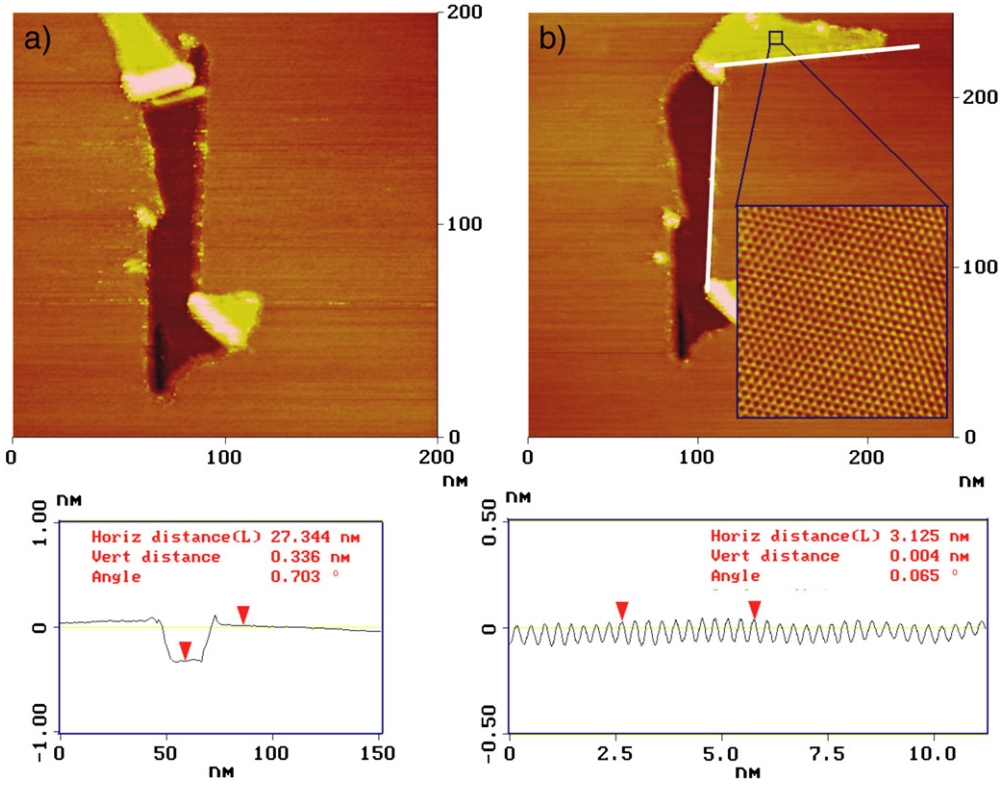

Fig. 3. STM images of a monolayer graphene flake cut by STL and back-folded during scanning (a). The line profile below the image shows that only the single atomic layer is moved. The back-folded graphene layer could also be rotated upon further scanning (b) to enclose an angle of 98° with the original zig-zag edge of the cutting. The atomic resolution image in the inset shows a Moiré-pattern of 0.31 nm periodicity as also evidenced by the line cut below.

atomic resolution STM images, see lower right inset of Fig. 3b and the corresponding line profile at the bottom. As apparent from Fig. 3b the two straight edges, before and after the folding out and rotation (marked by thick white lines in Fig. 3b), enclose an angle of 98°. The straight edge of the cut was oriented along a zig-zag direction. Using the well-known formula [37,40]: $D = na/[2\sin(\theta/2)]$,where D is the periodicity of the Moiré pattern, $n = 1,2,3,\ldots$ is an integer representing the rotation index, a is the periodicity of 0.246 nm of graphite lattice, an θ the misorientation angle, one obtains $D = 0.32$ nm for $n = 2$ and $\theta = 98°$, which is in excellent agreement with the measurements.

The position in which the folded out flake is stabilized is determined by two factors, the mechanical stress acting at the not fully separated edge of the folded out graphene flake and the energy of the Van der Waals interaction of the two layers. It was shown earlier by detailed theoretical calculations that the interaction energy of two graphene-like surfaces has a complex pattern of periodic minima and maxima, which may preferentially stabilize a certain angle of twist [41].

Scanning tunneling lithography can prove to be a useful tool for the controlled fabrication of twisted graphene multilayers with well-known misorientation angles, as exemplified in Fig. 3, as well as the detailed investigation of the resulting Moiré patterns. This will make possible the study of the ways in which the coupling/decoupling of the top layer(s) influences the electronic properties of purposefully designed, novel three dimensional (3D) graphene nanoarchitectures.

3.3. Parallel CTE

By its very nature CTE is better suited for parallel processing than STL, since in the case of the CTE process, a large number of hexagons can be grown simultaneously [29]. In the CTE procedure, first a localized defect region is produced by AFM indentation, see Fig. 4a. This defect region will define the location where the CTE reaction will start. This is a clear advantage of the CTE method as compared with the etching of graphene by nanoparticles [42–45], where the precise placing of the nanoparticles at a desired location is a highly challenging task [46,47]. As it can be seen in the line profile in Fig. 4a, the indentation modifies the SiO_2 under the graphene, too.

The versatility of the AFM in positioning the tip at a desired location makes it possible to produce an initial indentation pattern of

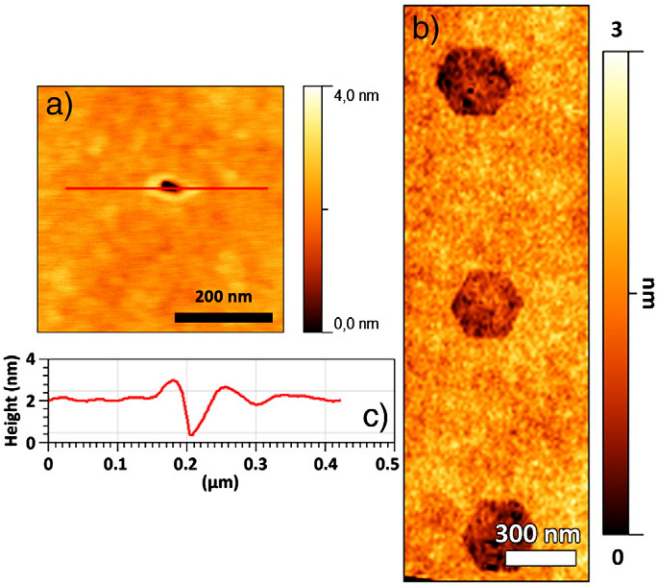

Fig. 4. Schematic of the AFM indentation. (a) A 2 nm deep indentation hole in a graphene layer. (b) A series of hexagonal etch pits produced by CTE, initiated by AFM indentation. (c) Line profile of the indentation hole.

high complexity, which, after the CTE, will yield a complex pattern of GNRs with zig-zag edges [29]. In a previous step to the indentation of a complex pattern the crystallographic orientation of the graphene layer has to be known. This can be achieved by a first CTE step on a single indentation that will reveal the orientation of the crystallographic axes.

The edge quality may be even better in the case of CTE than in the case of STL. While in the STL the edge is produced in a fast oxidation process far from equilibrium in the CTE the edge is produced during a slow, diffusion controlled oxidation process. As shown in Fig. 4b, all three hexagons have similar orientation and similar size. The solid phase diffusion process governing the extraction of oxygen from the substrate makes the reaction slow, therefore, the edges of a hexagonal etch pit move with a velocity of 0.21 nm/min [29], allowing for the precise control of the shape of complex patterns.

The multitip devices that will make possible massively parallel indentation for CTE are already commercially-available, like Dip Pen Nanolithography (DPN) [48].

3.4. Grain boundaries and CTE

Grain boundaries certainly will have an effect on the charge transport through graphene nanodevices if it happens that the nanodevice crosses a grain boundary. As during the primary oxidation phase (nitrogen–oxygen atmosphere, 500 °C) of CTE the oxidation starts in any defective region, this process is very useful to reveal the presence of grain boundaries, too. As shown in Fig. 5, AFM images clearly reveal the etched out grain boundaries. This will be very useful in deciding the location and the orientation of the devices to be realized in subsequent CTE steps. So, by a primary CTE process, one can reveal the grain boundaries present in the graphene flake and learn the crystallographic orientation of a certain grain, too. Then the subsequent indentation pattern can be designed in the most advantageous way. Carbothermal etching is the first process able to provide both of these pieces of information in a single processing step.

4. Outlook

Thinking further the possibilities of parallel nanopatterning also for scanning tunneling lithography, a custom designed system of isolated tips could be used in a matrix like it was used in the dot matrix printers. One tip of the matrix could be used for the operation of the feedback loop, while the other tips are used only during lithography on an atomically flat surface. Each tip should allow to be independently switched On/Off in lithographic mode, like in Fig. 6. In the present experiment both tips contributed equally to the feedback and the lithographic process.

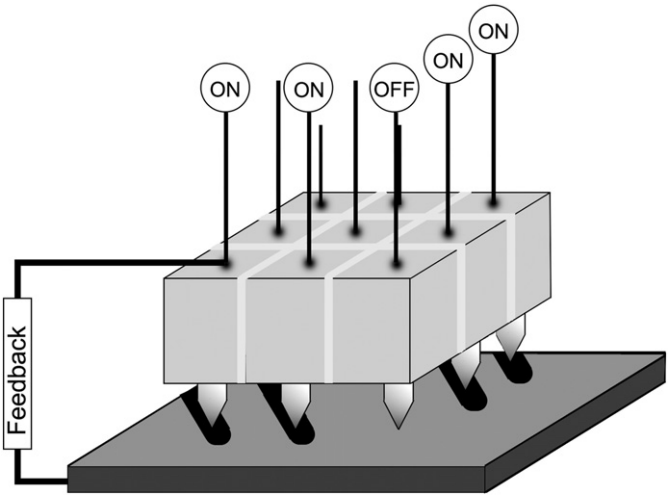

Fig. 6. Parallel STM tips, like a dot matrix printer.

The distance of independent and electrically isolated STM tips should be larger than 50 nm to avoid cross-talk between simultaneously etching neighboring tips. As a possible way to realize such multitip systems electrochemically produced Al_2O_3 membranes were proposed, which can act as a template for nanowire growth.

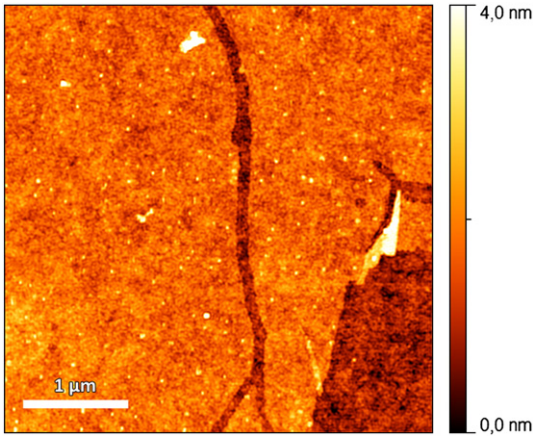

Fig. 5. AFM image of a graphene layer, supported on SiO_2, showing an etched out grain boundary.

5. Conclusions

Scanning tunneling lithography and carbothermal etching were compared under the aspect of the possibility of parallel processing needed nanoelectronic applications. Parallel processing is of utmost importance if practically relevant nanocircuitry from graphene is targeted.

Highly reproducible features were etched by STL along chosen crystallographic directions using a double STM tip showing that parallel processing is possible. Few layer graphene (FLG) systems with twisted orientation of the layers giving rise to Moiré patterns and tunable interlayer coupling dependent on the degree of misorientation of the individual graphene layers are coming into focus of attention. It is possible to produce such systems by STL, by cutting and folding out layers in a kind of graphene origami. This gives the opportunity to produce custom designed, 3D FLG systems with known orientations of the layers, whose novel properties can be investigated in great detail by atomic resolution scanning tunneling microscopy and scanning tunneling spectroscopy.

Carbothermal etching is even better suited for parallel processing than STL. After a first CTE step which gives information concerning the location of the grain boundaries and the crystallographic orientation of the chosen grain, complex patterns with precise crystallographic orientation can be etched following the AFM indentation at the points where the start of the CTE process is desired. Avoiding the crossing of grain boundaries is possible with this method. The multitip instruments needed for parallel CTE are already commercially-available as Dip Pen Nanolithography instruments with up to 55,000 tips.

Acknowledgments

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